	Qualification Test and Burn-in of Pixel Modules, Staves, and Sectors.		
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Qualification Test and Burn-in of Pixel Modules, Staves, and Sectors.

Abstract

This document describes the functional qualification procedure and test setups needed for this purpose. The description is not in sufficient depth to actually perform the tasks described. More detailed descriptions of particular items are given in the complementary documents ATL-IP-QP-0144 and ATL-IP-QP-0145. (see sub-documents).

Prepared by:	*Checked by:*	*Approved by:*
M. Garcia-Sciveres	**Pixel community**	**PDSG**

Distribution List

History of Changes

Rev. No.	*Date*	*Pages*	*Description of changes*
1	13/10/2003	All	Format and include various comments
2	15/10/2003	7,9,10,12	Changes/corrections following comments
3	16/10/2003	7,10	Changes following more coment

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1 Introduction

The pixel detector will not be operated as a unit prior to installation in ATLAS. Furthermore, once the detector is assembled, it will be very difficult, if not impossible, to repair or replace defective modules. Repairs become increasingly difficult and costly as components are integrated into modules, staves and sectors, barrels and disks. A production test program is therefore needed which detects faults at the earliest possible assembly stage. The full QA plan is outlined in the master documents ATL-IP-QA-0016 (for barrel) and ATL-IP-QA-0019 (for disk). The functional qualification testing is described in three complementary documents. This document provides a general description with a level of detail adequate for making a critical assessment and planning resource allocation. The document ATL-IP- QP-0144 "ATLAS Pixel Module Electrical Tests" spells out each functional test in detail, at the level required to actually perform the tests. Finally, ATL-IP-QP-0145, "Description of Data Analysis and Implementation of Selection Criteria For Atlas Pixel Modules", describes the data analysis process and how cuts are made to select modules for use in the detector.

Module functional qualification covers the necessary testing before and after modules are loaded on local supports. There are two basic goals: 1) to avoid loading defective modules or "weak" modules that will suffer infant mortality, and 2) to fully exercise each local support and test against all possible failures prior to integrating it into a larger structure. The first goal requires single module burn-in, while the second demands full stave or sector burn-in. While it is true that purely electrical infant mortality should occur during module burn-in, the thermal and mechanical configuration changes when a module is loaded on a local support, and mechanical stress induced failures of interconnects (bumps, pigtail) are not ruled out by module burn-in.

This document is intended to serve the following purposes. (1) Documentation for the production readiness review. (2) Guidance for assembly and loading sites regarding what hardware and software must be acquired and/or developed. (3) Determination of quantities and allocation of custom pixel test hardware, such as TPLL/TPCC sets. (4) Aid to managers planning what resources will be needed at each lab.

Where details are given for specific tests, such as voltages and numbers of events, they are current estimates based on I1 electronics and will possibly change as experience is gained with the I2 electronics. In any case the correct specification for each test is given in ATL-IP- QP-0144 and information in this document should be considered for information/planning only.

A conscious effort is made to separate specification of test procedures from acceptance decision making. Testing is taken to mean the accumulation of relevant data for each module, while acceptance cuts come later, during analysis of the stored data. Testing is regarded as a known quantity that depends primarily on specifications and module design, and can therefore be agreed upon and frozen early on, allowing uniform treatment of every module. Analysis of the data, on the other hand, is expected to evolve until well into production, because in order to reject "abnormal" modules, one must first know what is "normal", and for this one needs a uniform data set from a significant number of modules.

Important points follow from this conscious separation of testing and analysis. (1) Every module must be fully tested- there are no branch points where the test sequence is aborted. (2) Large quantities of data must be stored and managed, rather than pass/fail test results. (3) Acceptance cuts will be made by running an analysis program on stored data.

2 Qualification Requirements

2.1 Bare Modules

The purpose of bare module qualification is quality control of the flip-chip operation, leading to acceptance of the bare module or its return to the vendor for rework or credit. The expense and effort invested in the flex hybrid plus MCC that must be added to the bare module in order to make an assembled module are very small compared to the bare module itself, so a very detailed characterization of the bare module is not warranted. The bare module testing is therefore a single chip FE probing test, plus a sensor IV test.

2.2 Modules

Assembled modules must be qualified before they can be loaded on local supports. This is the first chance for each production assembly to be operated as a complete module with full functionality. This must therefore be a comprehensive test verifying all aspects of module operation and producing configuration files describing the module "personality". Selection cuts to determine what part of the detector the module is suitable for will be based on the measurements made on these tests (for example, the modules with the least number of bad pixels should be used in the B layer). Apart from selection cuts based on measurable quantities such as number of bad pixels, before they can be loaded on local supports, modules must be proven capable of stable operation in realistic conditions. The modules must therefore be burned-in, as well as characterized at operating temperature. Unfortunately "operating temperature" is not a precisely defined quantity, so module properties must be stable as a function of temperature. The approach to testing temperature stability is to carry out some tests at different temperatures. The temperatures chosen at 30C and −10C as measured by the module NTC.

Other than electrical tests, the modules must be visually checked for damage, and measured to fit within the allowed envelope. A final aspect of qualification involves the wire bonds, which can be checked through sample destructive pull tests at this stage and through sample accelerated aging after the module is removed from its flex frame.

2.3 Staves and Sectors

The function of the local supports is to precisely hold the modules, provide cooling, and support services. The modules mounted on a local support must function fully as measured at the single module level (prior to loading on local supports), so enough tests must be run in order to verify that the modules operate as expected. The operating temperature must be controlled and stable with all modules powered and running. The performance of each module must be stable over time with all modules running. The module integrity and position must be stable with thermal cycling.

3 Test Setups

3.1 Bare Module Test Setup

The bare module test setup combines elements from the Module Test Setup, described below, and the FE chip probing setup, which is beyond the scope of this document. The bare module stetup is discussed further in ATL-IP- QP-0144.

3.2 Wire Bond Test Setup

Performing bond pull tests requires a wire bond pull tester. This equipment should be available at each of the module assembly sites. Wire bonds will also be pulled from the empty frame after aging. This will require an oven and a pull tester at the local support loading sites. Alternatively, empty frames could be returned to a module assembly site promptly after separating the module from the frame.

3.3 Module Test Setup

A module test setup has evolved over the years and has become a standardized element if Pixel Collaboration institutes. The official technical description is given in a separate document: ATL-IP-ES-0088 "Pixel Module Test Setup Specification". The narrative description of the elements is given below, with explanation of what they used for.

3.3.1 Cooling

A liquid cooling system is not required to operate single modules. Adequate cooling is provided by simply placing the base of the module frame carrier in contact with a metal heat spreader. Typical module temperature with such an arrangement is 10C above ambient. The module and heat spreader can in turn be placed in an environmental chamber or simple cold box with dry nitrogen flow to implement cold operation. Either an environmental chamber or a cold box with dry air is required for the module test setup. The cold environment should produce –10C measured on the module NTC.

3.3.2 Electrical Hardware

The official description of the electrical hardware is given in ATL-IP-ES-0088. In general terms, the setup uses a PC computer with VME and GPIB interfaces, a VME crate with a custom board denominated Turbo PLL, and external custom board denominated Turbo PCC, and GPIB-controlled off-the-shelf power supplies.

3.3.3 Radioactive Source

To properly assess the response of each pixel and perform an absolute calibration a radioactive source scan will be necessary. Also, while finding disconnected pixels has been possible through noise scans and bias-off scans, there is not at this time a widely accepted method that can substitute a source scan with 100% reliability. The radioactive source used should be Am^{241}, filtered to give a 60KeV peak suitable for absolute calibration. The activity should be such as to provide a minimum of 20 hits in every pixel within a reasonable test time. Safeguards, and implementation will vary from site to site depending on local procedures and regulations. Irradiation is possible from the top, through the flex and surface mount components, or from the bottom, through the FE chips. Bottom irradiation is more uniform and therefore requires less source activity. However, as long as the 20 hit/pixel minimum is satisfied, labs are free to pick the most practical source placement.

3.3.4 Software

The module test software is known as TurboDAQ. The latest version should be used. A batch mode capability is additionally needed for production, such that a sequence of tests can be executed automatically. This capability may become part of TurboDAQ itself, or a new layer of code may be developed that calls TurboDAQ for each individual test, similar to the FE chip probing software. Either way some additional software development is needed for production use, but this additional development is considered minor compared to what already exists.

3.4 Module Burn-in Setup

3.4.1 Cooling

An environmental chamber is required for this purpose, since the module environment temperature must be capable of automatic cycling between the extremes of +30C at and –30C (this is the environment temperature, not the NTC temperature). The NTC temperature will range between –30C (with module power off) and near +40C (with module power on). The chamber should be large enough to fit several modules at the same time (number of modules depends on the assembly rate at a given site).

3.4.2 Electrical Hardware

The burn-in setup is built on the TurbDAQ setup described under Module Test Setup, with appropriate added components to fill the burn-in requirements of long term unsupervised operation of multiple modules in tandem. The required components are:

1) PC computer with VME interface and USB port, and sufficient disk space (see Data Handling section)
2) VME crate/mini-crate with Turbo PLL board (existing)
3) Turbo PCC board (existing)

4) Burn-in adaptor boards (known as SURF board). 1 board for every 4 modules of burn-in capacity, up to 16 modules maximum.
5) +5V & -5V power supply for PCC, and +5V supply for SURF boards (can be same +5V supply).
6) +3V to +4V, 24A DC, dual bulk supply for module current. This supply will be constantly on and does not need any remote control capability. Multiple smaller supplies (dual 6A per SURF board) can be used instead.
7) ISEG high voltage supplies, 1 for every 9 modules.
8) +24V DC supply to power ISEG supplies.

3.4.3 Alarms and Limits

Since the modules during burn-in will operate unattended for long periods of time, the setup must provide protection against damaging conditions, such as overtemperature, overvoltage, and overcurrent. Such limits will be implemented in hardware on the SURF burn-in board. The module temperature should never be allowed to exceed 40C.

3.4.4 Software

Development of control software for the burn-in setup is in its infancy (8/2003). Significant work is needed to have a working system. The software must keep track of multiple modules through thermal and power cycling, performing periodic tests. The tests themselves will be accomplished by calling TurboDAQ. In addition to the data generated by TurboDAQ calls, the new software must continually record temperatures, voltages, and currents, and must respond to limits and alarms. The hardware allows reading voltages and temperatures on all modules simultaneously. However, TurboDAQ data acquisition is possible on only one module at a time, while the rest of the modules can still be powered and operated- just not read back.

3.5 Stave and Sector Test Setup

3.5.1 Cooling

A local support with all modules powered can only be cooled by flowing coolant through the cooling circuit. An evaporative system is not required for qualification testing. Liquid coolant with a chiller capable of –30C will be the most convenient in general. The cooling tubes must be properly cleaned after use with liquid coolant. This will be accomplished by flushing with distilled water, followed by vacuum drying and nitrogen purge.

3.5.2 Environmental Protection

Since the coolant temperature will likely be below the dew point in test labs, the sector or stave under test should be in a test box with nitrogen flow and adequate feed-throughs to prevent condensation on cooling and electrical connections.

3.5.3 IR Imaging

Since the temperature sensor on the modules does not provide individual chip information, an IR image with sufficient resolution to see each FE chip will be necessary in order to assess the quality of the thermal contact. Most likely the imaging will have to be done with the parts exposed to ambient air. Therefore the cooling should be adjusted so that the temperature of the coolant is above the dew point, but the temperature of the modules is not above 35C. This may require a humidity controlled room. The purpose of the IR image is to establish the temperature uniformity of modules and not the absolute temperature. Therefore the reflectivity of the modules is not critical.

3.5.4 Electrical Hardware

The electrical testing of local supports is not completely decided at this time (8/2003), and will likely evolve as experience is gained with prototypes. To be safe, we assume this setup will be the AND combination of the module test and burn-in electrical hardware sets. The module burn-in setup capabilities are necessary to operate all modules on a local support at once, while the test setup capabilities might be necessary to verify that the performance is the same as before loading on local supports. It is possible that with time, the module

burn-in hardware might be capable of supporting most, if not all the qualification tests. However, this can certainly not be assumed at this time, before all the burn-in components even exist. All parts of the "safe" setup already exist or will be ready for the start of module production. Operation is a known quantity.

It may also be desirable to operate a fully loaded local support with a ROD. We are investigating if this would be possible without schedule penalties. Apart from the ROD and crate themselves, this will require (1) a PP0 adaptor board (or 2 for a stave) (2) power supplies- perhaps a crate of the production supplies, in which case also a PP2 regulator box. (3) a control system for the power supplies. As with the module burn-in system, at this time it cannot be assumed at this time that all the necessary performance tests to be compared with single module data could be performed with a ROD setup.

3.5.5 Radioactive Source

Connectivity of bumps must be checked following thermal cycling of local supports, which will put the greatest mechanical stress on the modules. If no reliable alternate method is available for identifying disconnected bumps, then a radioactive source must be part of the sector/stave test setup. There is no strict requirement on isotope since no calibration peak is needed, but the energy and activity must be high enough to "see" through the surface mount components, as irradiation in this case can only be done from the top.

3.5.6 Software

In the case of the TurboDAQ "safe" setup the same software as for single module testing is required. Operation with a modified burn-in setup only would require additional software, for example to perform a sensor IV scan using the ISEG supplies instead of the Kiethly GPIB supply. Such software development represents a moderate effort. ROD operation requires more extensive software development, some of which is common with the on-going software development for ROD operation in the actual experiment.

3.6 Stave and Sector burn-in Setup

3.6.1 Hardware

Since a stave or sector is already a parallel assembly of modules, the test setup can be used for burn-in as well. The system used for cooling will require remote control capability in order to implement thermal cycling, which is not a significant complication. Active heating should not be required for thermal cycling, as the module heat load should be sufficient to quickly bring the temperature up to the +40C extreme as the cooling is switched off. Some cooling might still be necessary to prevent the temperature from rising too fast or overshooting. For reliable, safe operation, it may be necessary to add a heater to the input cooling line as a means to vary the cooling capacity, rather than changing the chiller temperature. This again is not a major complication.

3.6.2 Software

Small additions to the test setup software will be needed to implement burn-in. Chiller/heater control, continual recording of temperatures, implementation of alarms and interlocks, etc. Other than chiller control, the module burn-in software should work well for stave/sector burn-in using the TurboDAQ setup.

3.7 Number of Setups

A very crude estimate of the minimum number of setups required to build a 2 (3) hit pixel detector is presented. The number of modules to be tested includes yield loss and spares, and is taken to be 1275 (1930). We also assume that the efficiency for using any given setup is 70%, including ramp-up and down-time. For assembled module testing, we assume each module requires a full 8-hour shift, and test setups are operated for only one shift per day. Thus, a 220 day production schedule would require 9 (13) setups. For burn-in, assume 2 cycles per week and 10 modules per setup average load. Thus, a 50 week production would require 4 (6) module burn-in setups. Finally, for stave and sector test and burn-in, 1 setup per loading site (3 stave sites + 1 disk site) is sufficient, allowing 1 week use per local support. If all setups are based on Turbo PLL/PCC, this implies that 17 (23) sets are required for production module and local

support qualification. This does not include spares or additional inefficiencies from geographical distribution.

4 Overview of Tests

4.1 Electrical Measurements

The items described in this section are not necessarily individual tests, but rather areas in which measurement data are required. Each item listed may come from a dedicated test or from a combination of data from one or more less specific tests. A detailed description of the actual tests is given in ATL-IP-QP-0144. The order in which the items are described is also not necessarily the order in which information is collected. For example, the "Monleak scan" of the Sensor Bias item is not very sensible before the module has been tuned. On the other hand it is advantageous to perform the IV scan and determine the bias set point before tuning. Finally, the description of test items is decoupled from the question of operating temperature, which will be considered in the "Qualification Sequence" section.

4.1.1 Power

Current and voltage measurement for each power supply at nominal value and in voltage corners (see "Operating Margin" below). A scan that measures quiescent and operating currents individually for each FE chip should be run for the standard current measurement. Currents should be monitored during all subsequent tests and alarms and limits should be implemented. During burn-in, the power test should include 10 on/off cycles.

4.1.2 Digital Functionality

Must check all registers and all buffers using digital injection to test full and overflow conditions. Test all pixels with digital injection (digital inject scan). Must do this at nominal VDD at 40MB/s single link. 80MB/s single link, 40MB/s dual link, and 80MB/s dual link. Digital scans that record no errors need not be saved, but if not saved then a record must be kept that the scan was performed.

4.1.3 Operating Margin

This should measure the voltage range over which a module operates correctly. The digital and analog voltage limits should be measured separately. For the digital voltage, a digital scan should be performed in steps of 100mV above and below nominal, until errors are recorded. The last error-free scan gives the voltage limit, and only the first error-reporting scan need be saved (along with the voltage and current readings). While in principle only the digital supply voltage is being varied, the analog voltage may have to be varied as well to avoid exceeding a diode drop between the two supplies. This test should be performed both in dual 80MB/s mode and single 40MB/s mode. A reduced digital scan optimized for speed might be desirable. Not all pixels should have to be read out to detect errors.

Once the VDD operating margin has been established, the frequency margin should by running 40MB/s single and 80MB/s dual scans at 50MHz TPCC clock, nominal voltage. If errors occur the san(s) should be repeated at 45MHz.

The analog voltage limits will be harder to determine, as scans take longer and one should look not so much for hard errors but rather for performance degradation. To make this test practical, analog scans should be performed at only the two extremes VDAA=2V and VDDA=1.4V. The lower extreme will require lowering VDD to below nominal. If the scans proceed with no errors, that concludes the test. If there are errors in either scan, the alternate extreme of 1.8V or 1.5V should be used for the scan(s) that failed. All data must be saved. Only dual 80MB/s mode is needed.

4.1.4 Sensor Bias Voltage

A Sensor IV scan must be performed up to 600V. The compliance of the supply must be set to something safe for this test. 100uA is the nominal starting point, but this may be adjusted with further experience. Following the IV scan the operating point for the module should be set to 50V below the breakdown voltage, or 550V, whichever is less. This voltage should then be used for all future tests requiring

bias, in order to accumulate time at the highest possible voltage. Immediately following the HV scan and the set point selection, a Monleak scan should be performed.

4.1.5 Analog Functionality

This is the most complex measurement to be performed. There is a sequence of operations and scans needed to certify proper analog behavior and to tune the module for subsequent use. The sequence of analog tests is roughly as follows:

a) Import Capmeasure data from FE wafer probing
b) Threshold tune (TBD if using internal or external injection or both)
c) Internal injection threshold scan
d) External injection threshold scan
e) FDAC tune and test
f) Cross-talk scan
g) Time-walk scan

In-time threshold scan

h) In-time threshold scan in voltage corners
i) TOT scan

4.1.6 Noise Occupancy and Hot Pixels

This is needed to set a baseline for what the quiet module looks like that can then be used as a reference for multi-module tests on a local support, where external noise may be present. A map of hot pixels is additionally necessary to carry out a source scan. Two hot pixel masks are to be generated, a fast and a slow. The fast mask should be adequate for realistic LHC operation, while the slow mask will be needed for source scans. The difference between these two masks might also be of interest for acceptance cuts.

The test consists in enabling one FE chip at a time in self-trigger mode and "waiting" for hits. Pixels that generate hits at a rate greater than 1Hz (1KHz) should be flagged as hot and disabled in the slow (fast) mask. With the HitBus scaler function in FE-I2, this type of scan can be fully automated.

Additionally, it will be necessary to look for noise occupancy that is caused by activity in the module itself. A new type of scan is proposed for this, which is essentially a threshold scan where, with every mask step, one counts only the hits in the pixels that were not injected. For a typical scan, each mask step looks at 16 crossings, times 200 VCal settings, times 100 events, or about 3x10-5 crossings. Therefore, a threshold scan with 1000 events would allow catching hot pixels at the required level.

4.1.7 Source Scan

Record >20 events in every pixel. Measure source energy spectrum

4.1.8 Source-less Bump Continuity

This consists of two internal injection analog scans with bias on (150V) and the other with bias off. Additional refinements might be added for better sensitivity to indium bump opens.

4.1.9 Slave Operation

No data is produced by this activity. It is simply a way to operate the module realistically for an extended period of time, necessary for burn-in. There are two possible operating states for the burn-in system: (1) a scan is being performed on a given single module with data being recorded, and (2) no data is being recorded from any module. During condition (1), all other modules under burn-in can be exercised in the exact same way as the module being scanned, but the output data they produced is not recorded. During condition (2) modules could be placed in a self-trigger mode with a very low threshold so that they will have random hit activity, or an indefinite scan loop could be run without recording the output data from any module. Note that

turning off the sensor bias in order to increase noise and generate more hits is not an option because bias voltage burn-in is taking place at the same time as chip operation burn-in.

4.2 Mechanical and Thermal Tests

These are individually included in the Assembly Breakdown Structure, and referenced in the master QA documents ATL-IP-QA-0016 and ATL-IP-QA-0019. The tests are listed below with some comments.

4.2.1 Surveys

4.2.2 Visual Inspections

4.2.3 Wire Bond Pulls and Accelerated Aging

4.2.4 Temperature measurements

IR imaging checks that every FE chip is in good thermal contact to the local support. It does require cooling, but the coolant will be above the due point to avoid the difficulty of implementing IR imaging inside a cold box. An electrical Idle test will be run for the duration of the imaging process.

4.2.5 Thermal Cycling

This is both a “stress test” to weed out weak parts that might be prone to infant mortality as well as a simulation of environmental conditions the parts will see during long-term operation. Single modules can be cycled in an environmental chamber, while local supports can be cycled in their dry box with liquid cooling. While cycling without module power should produce the required mechanical stress, cycling powered modules is a more realistic simulation of operation and is therefore preferred. The temperature range should be –30C to between +35C and +40C measured at the module NTC (note that +40C is the trip limit, so the upper set point for cycling should be enough below 40C to avoid spurious trips), with at least 30 minute dwell time at each temperature for any stress build-up to have an effect. The number of cycles is to be determined. The basic testing that accompanies thermal cycling is detection of any induced changes. For example, while it is acceptable and likely normal for a module to have a few disconnected bumps, if just one bump is seen to be disconnected after thermal cycling, but was connected before, this could indicate a serious weakness and should immediately raise a red flag. Similarly, changes in a local support IR image (which shows relative chip temperatures) should raise a red flag. The actions to be taken in these cases will depend on experience as statistics for this test accumulate. It is not known at this time (10/2003) if there is some “infant mortality” effect for a few bumps to become open or module to local support thermal contact to relax. These issues will only be well understood with significant statistics.

5 Test Sequence

5.1 Assembly Tests

All parts should undergo visual inspection before assembly and any features (such as sensor scratches) should be recorded and tracked. Also sensor ID marks should be checked and recorded just prior to module assembly, as they will no longer be visible after assembly. When gluing components, samples of the glue mix used should always be cured and checked to verify that proper curing took place. Other assembly tests involve wire bonds. Immediately before wire bonding each module, 10 wire bonds on the flex test region should be pull tested. These bonds should have been made with the same settings to be used for the FE chip bonding. This test will provide immediate feedback in case of a change in conditions. After a module is removed from its frame and loaded on local support, the frame should be subjected to accelerated aging at 200C for 24 hours. The test bonds on flex test area (which remains behind on the flex) should be pulled after this. This step can take place at the module stave loading or module assembly sites (the empty frames can be returned to module assembly sites). Note that since the aging test takes time (even without shipping back to module assembly sites) this test will not prevent one for loading a module with a aging problem on a local support. However, the

purpose of this test is not to prevent aging problems: it is simply a quality control check to guarantee that there will be no aging problems Such problems are prevented by proper wire bonding practice an by avoiding chlorine contamination, and more of the empty frame aging tests are expected to yield diminished pulls. .

5.2 Initial Electrical Test

The purpose of this test is to check that the module has been assembled correctly. And has adequate performance to run through the rest of the qualification. Additionally, the module must be characterized in sufficient detail to be certain that changes induced by burn-in (including thermal cycling) can be detected. These tests can take place at room temperature, leaving cold operation until after burn-in. While it might seem better to have comparison data taken under exactly the same conditions before and after burn-in, recall that module operation must be stable with temperature, because operating temperature is not fixed, and therefore comparing “warm before” to “cold after” is a more powerful stability test, while it is also more practical. Should any discrepancy be detected by such comparison, one can always repeat room temperature tests after burn-in in order to disentangle it.

5.3 Module Burn-in

This test consists of running the module under various conditions for a period of 48 hours. Since the module temperature will be cycled this test should be performed in an environmental chamber. There is no proper cooling circuit with feedback and interlocks. What is controlled is the ambient temperature, and the module temperature will depend on whether the module is powered or not, and how good the thermal contact is. The module temperature should be monitored throughout the burn-in via the NTC, and the burn-in hardware should trip the power if it exceeds 40C. While at low temperature, the module should be powered-off for approximately 10% of the time (this will allow it to actually reach –30C). Tests to be performed are Power every time the temperature is changed, followed by analog tests to monitor potential evolution of quantities of interest, such as noise, threshold, and dispersion. All other times the module is powered it should be in a slave state. The bias voltage should be kept at the set point determined by the HV test and bias current should be monitored and recorded at all times.

5.4 Full Electrical Characterization of Module

At the end of the burn in period the module should be fully characterized at nominal operating temperature (-10C).

5.5 Module Receiving Tests

When a module is shipped to a loading site it cannot be assumed that nothing happened during shipping. On the other hand it will generally not be possible or practical to repeat the final tests at the loading site. Instead, a reduced set of tests will be performed to provide confidence that the module was not damaged in shipping. These tests can be performed at room temperature.

5.6 Initial Loading Tests

This test can be performed without cooling. Its purpose is to check that the delicate module circuitry survived the loading operation, providing fast feedback. Since there is no cooling, modules should be powered one-at-a-time and only for a short time. The question on whether to perform this test in “real time” as each module is loaded, or just once after all modules have been loaded, will depend on practical details of the

loading operation, and of course on the yield of the loading process. Since loading is designed and qualified to have negligible yield loss, it should in principle not be necessary to test in "real time". However, only experience will show if this is borne out, and so the possibility of real time testing should be entertained in production loading plans.

5.7 Pre-Burn-in Inspection of Stave and Sector

IR image

5.8 Stave and Sector Burn-in

Primary purpose is thermal cycling. Electrical components have already been burned-in in the conventional use of the term.

5.9 Post-Burn-in Inspection of Stave and Sector

IR image

5.10 Electrical Test of Stave and Sector

Individual modules will have been tested and burned-in prior to loading on the local supports. The aims of the electrical test of the stave or sector are (1) to check that no subtle changes occurred during loading and (2) to verify stable performance under simultaneous operation of all modules. The stave or sector will have to be kept in a dry box and actively cooled for most of these tests. The nominal module temperature shall be –10C measured at the NTC.

6 Data Handling and Storage

The electrical tests generate large amounts of data per module. These data should be stored and backed-up locally at the test institutes. The responsibility of implementing local backup must be stressed. In addition to storing the original test data, the information shall be read into Module Analysis Framework (the module data analysis environment) and stored as a root file on a web-accessible page, together with the TurboDAQ module configuration files. The URL pointing to this stored information should be entered into the Production Database (PDB). It is the testing institute's responsibility to update the PDB should the web address of the stored data change.

7 Data Analysis and Selection

An automated method to apply a standard set of quality cuts is required. This will be implemented in the Module Analysis Framework, with the actual cut values defined after experience with the I2 version of the electronics. The framework, data analysis process, and cut methodology are described in ATL-IP-QP-0145.